IMPLEMENTATION OF CONTINOUSLY CONTROLLED STATIC VAR COMPENSATOR FOR POWER FACTOR CORRECTION SYSTEM USING PSPICE

Karthick G A[1], Ramesh V[1], Sundar Ganesh C S[2]

[1]UG student,Department of EEE, PSG College of Technology, Coimbatore,India

[2]Assistant Professor, Department of Robotics & Automation, PSG College of Technology, Coimbatore, India

Abstract

In an electric power system, a load with a low power factor draws more current than a load with a high power factor for the same amount of useful power transferred. The higher currents increase the energy lost in the distribution system, and require larger wires and other equipment. Because of the costs of larger equipment and wasted energy, electrical utilities will usually charge a higher cost to industrial customers where there is a low power factor. The inductive loads constitute major portion of the power consumed in industrial complexes. Reactive power required by inductive loads increases the amount of apparent power in the distribution system. This increase in reactive and apparent power results in a larger angle and hence results in low power factor. There are many advantages of maintaining high power factor which include elimination of penalty billing, increased system capacity, increased voltage level etc. The proposed methodology employs a thyristor switched-capacitor bank to generate a controllable static VAR for single phase AC system. The capacitor bank is constructed of five binary weighted thyristor-switched capacitors. This arrangement leads to a capacitor bank capable of generating stepping reactive power having thirty one equidistant non-zero levels. Each capacitor is controlled by a single thyristor shunted by a reverse diode. The system is capable of correcting lagging power factor up to unity or adjusting it according to user desire. Each capacitor is connected to a series reactor for protecting the solid state combination from inrush current occurring at the first instant of compensator plug in to power system network.

Keywords— Power factor improvement, Thyristor control, PSPICE, Capacitor Bank, Energy utilisation

1. Introduction

The power factor of an AC electric power system is defined as the ratio of the real power flowing to the load to the apparent power in the circuit, and is a dimensionless number between O and 1. Real power is the capacity of the circuit for performing work in a particular time. Apparent power is the product of the current and voltage of the circuit. In an electric power system, a load

with a low power factor draws more current than a load with a high power factor for the same amount of useful power transferred. The higher currents increase the energy lost in the distribution system, and require larger wires and other equipment. Because of the costs of larger equipment and wasted energy, electrical utilities will usually charge a higher cost to industrial customers where there is a low power factor.Thyristor Switched Capacitor controlled by help of programmed microcontroller where it is depicted that the power factor can be improved to unity with light loading and can be maintained to around 0.98 with increase in system loading [1].

Capacitor bank connected in shunt helps in maintaining the power factor closer to unity. They improve the electrical supply quality and increase the efficiency of the system [2]. The automated power factor corrector (APFC) using capacitive load bank is helpful in providing the power factor correction. Proposed automated project involves measuring the power factor value from the load using microcontroller [3]. An indigenous technique and method which could be used for static power factor correction. It is demonstrated in this work that phase difference between voltage and current can be determined using zero crossing detectors, opto-couplers, EXOR gate and some basic function of Arduino microcontroller[4]. The system deals with the implementation of automatic power factor correction system using solid state switched capacitors and Arduino UNO controller [7]. The main causes of low power factor are inductive loads which include induction motors, transformers, induction generators etc. These inductive loads constitute major portion of the power consumed in industrial complexes. Reactive power required by inductive loads increases the amount of apparent power in the distribution system. This increase in reactive and apparent power results in a larger angle 8 and hence results in low power factor. There are many advantages of maintaining high power factor which include elimination of penalty and reduced peak kW billing demand, increased system capacity, increased voltage level etc., so it is essential to improve the power factor in industrial sectors. A poor power factor for the plant causes huge amount of losses, leading to thermal problem in switchgears [5]. This system is implementing a new technology for power factor improvement of 3 phase induction motor [6].

Fig.1 shows the capacitor bank configuration of the proposed system. It is composed of five binary weighted capacitors. This configuration offers 31 non-zero levels of possible capacitive reactive current. Each capacitor is controlled by a single thyristor shunted by a reverse diode. The thyristor handles the positive half cycle of the capacitor current and the diode deals with the negative half cycle. Reactors LS1 to LS5 are current limiters.

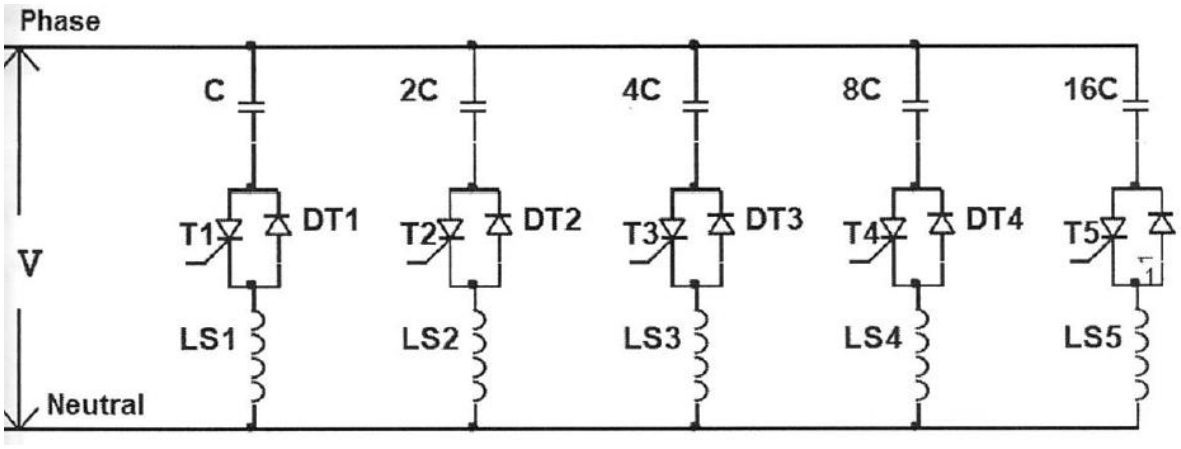


Fig.1 Capacitor bank configuration

2. Methodology

The proposed methodology employs one thyristor switched-capacitor bank to generate a controllable static VAR for single phase AC system. The capacitor bank is constructed of five binary weighted thyristor- switched capacitors. This arrangement leads to a capacitor bank capable of generating stepping reactive power having thirty one equidistant non-zero levels. The controlling circuit of the capacitor bank is designed such that maximum absolute deviation from linear response is 1/62 of its rating. Each capacitor is controlled by a single thyristor shunted by a reverse diode.

Fig.2 shows the block diagram of the proposed single phase power factor correction system. The capacitor bank triggering circuit is excited by two signals. The first signal is KiL, where K is the attenuation factor of the current transformer (C.T) circuitry and iL is the instantaneous load current. The second signal is K*v, where K* is the attenuation factor of the voltage transformer (V.T) circuitry and v is the instantaneous phase voltage. The load voltage and current can be given by Eq.(1.1) and Eq.(1.2).

$$v = Vm \sin(wt) \qquad \text{-- 1.1}$$

Where, Vm is the load voltage amplitude in volts,

t is time in seconds.

The first zero-crossing detector in Fig.1.2 converts K*v to a rectangular waveform (V1}, which is then differentiated and half-wave rectified by the first RC differentiator/rectifier, forming V2. The latter is a train of pulses used to trigger the sample and hold circuit at wt = mr, where n is a positive odd integer. The analogue differentiator converts K*v to the analogue signal V3 which is then zero-crossing detected, forming the waveform V4. The latter is processed similar to V1, forming VS.

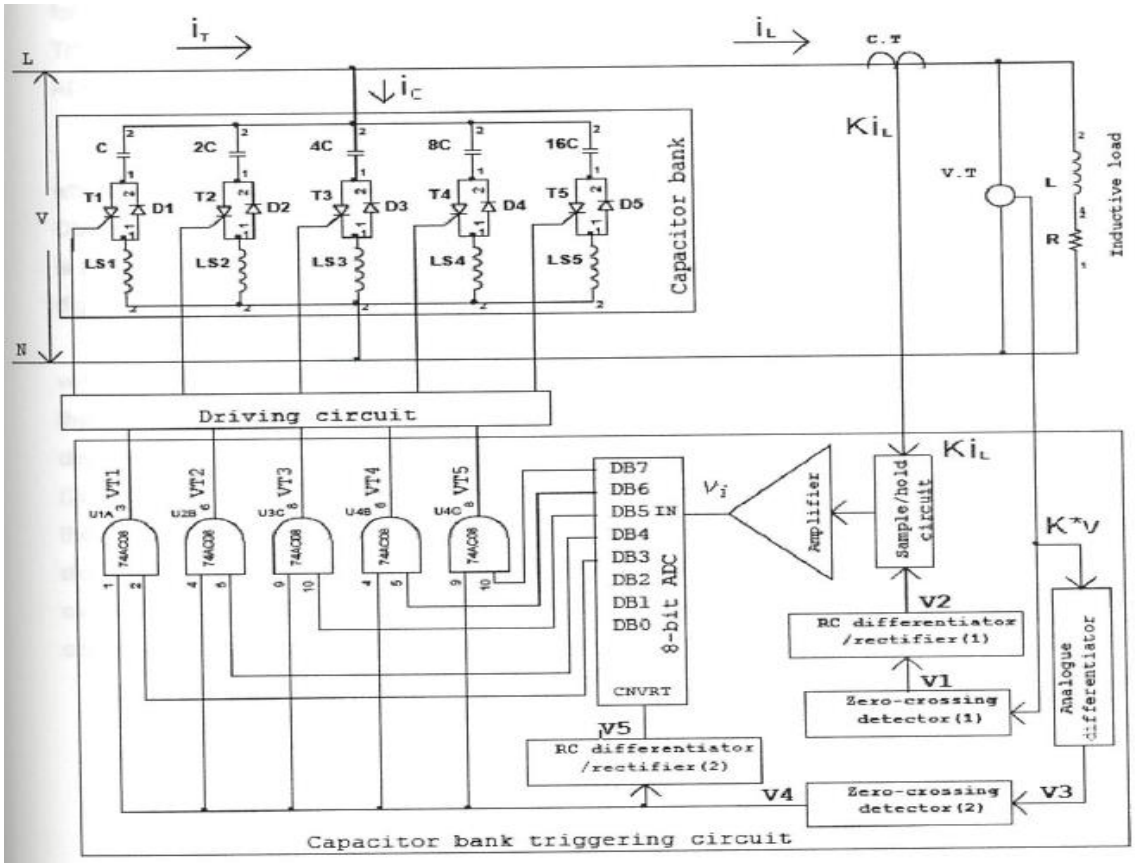


Fig 1: Block diagram of the proposed single phase power factor correction system

The current signal KiL is sampled by the sample and hold circuit at wt= mr, where n is a positive odd integer, yielding an analogue signal proportional directly to the reactive current component of the load current.

The latter signal is amplified and clamped upward by 0.15625 volts producing the analogue voltage Vi which is proportional to the reactive current demand. Vi is the analogue input of the 8-bit analogue-to-digital converter (8-bit ADC) . For unity power factor correction and at full compensator rating, Vi will have a magnitude of 10 volts. The 8-bit ADC starts conversion at wt = (2n-1)TT/2, where n is a positive odd integer. The five most significant digits (DB? DB6, DBS, DB4, and DB3) of the 8-bit ADC are employed for controlling the capacitor bank switching devices (TS, T4, T3, T2, and T1) respectively.

when Vi is zero, all the digital outputs of the 8-bit ADC are logic zero. When Vi is 10 volts, all the digital outputs are logic one.The driving circuit includes five sub-circuits; each one of them deals with one of the thyristor (T1 to TS). Choosing appropriate switching instants will protect the switching devices from inrush currents. The appropriate switching of thyristor occurs at wt = (2n+1)rr/2, where n is a positive odd integer. At these instants dv/dt is zero and each of the capacitors (C, 2C, 4C, 8C, and 16C) is charged to -Vm through its corresponding diode and limiting reactor.

3. POWER CIRCUIT

The power circuit is shown in Fig.3. It consists of one thyristor switched-capacitor bank to generate a controllable static VAR for single phase AC system. The capacitor bank is constructed of five binary weighted thyristor- switched capacitors. This arrangement leads to a capacitor bank capable of generating stepping reactive power having thirty one equidistant non-zero levels. Each capacitor is controlled by a single thyristor shunted by a reverse diode. The thyristor handles the positive half cycle of the capacitor current and the diode deals with the negative half cycle. Reactors connected in series with the capacitors are current limiters. Choosing appropriate switching instants will protect the switching devices from inrush currents. The appropriate switching of thyristor occurs at wt = (2n+1)rr/2, where n is a positive odd integer. At these instants dv/dt is zero and each of the capacitor s is charged to -Vm through its correspond ing diode and limiting reactor.

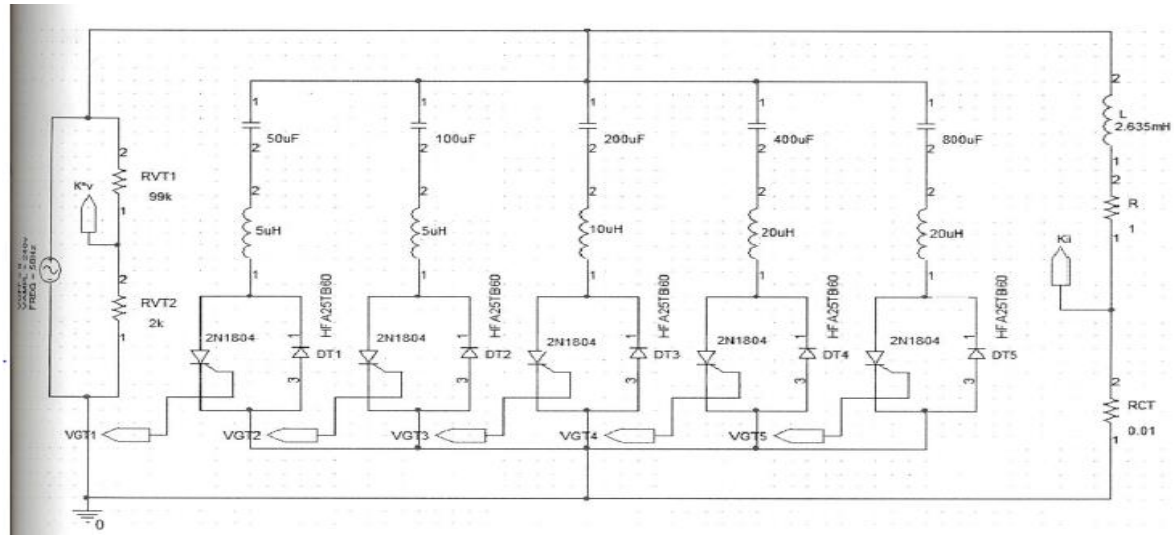


Fig.3Power circuit

3.1 THYRISTOR GATE TRIGGERING CIRCUIT

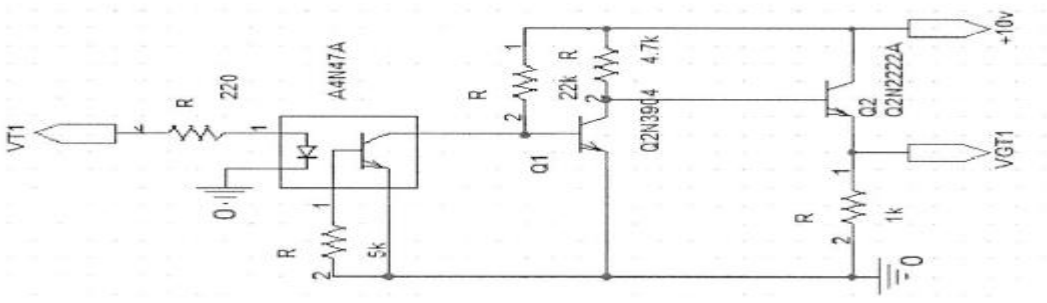


Fig.4 Thyristor Gate Triggering Circuit

Fig.4 shows the gate triggering circuit of thyristor T1. The output from the ADC is applied to the voltage comparator, then to the AND gate and then to the voltage follower. The output from the voltage follower is VT1, which is shown in Fig.3.6. From Fig.3.5, VT1 is applied to the opto-coupler. When VT1 is logic high, opto-coupler is turned on and the transistor 01 is turned off and hence the transistor 02 is turned on. Therefore, there i a voltage drop across 1K resistor which supplies the gate voltage of thyristor T1 and the thyristor T1 is turned on.

4. Simulation and Results

All the designs are tested and validated using Cadence Orcad PSpice software. This simulation tool helps in testing the validity of the design and also save cost by reducing the chances of error. Any defect in design can be easily identified and rectified well before the implementation, thus saving cost and time.

SIMULATION RESULTS

Simulation of zero crossing detector 1

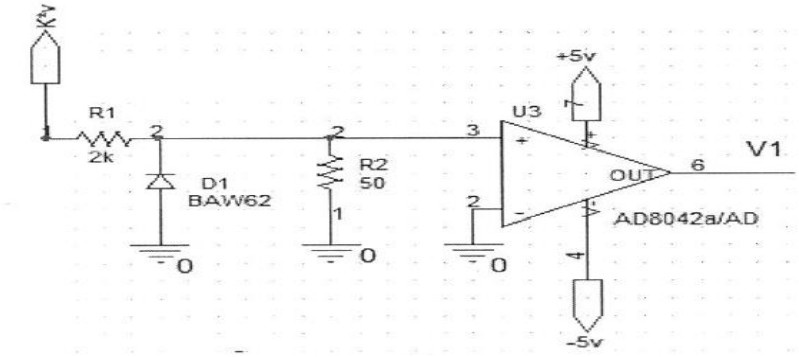


Fig.5 Simulation of PSpice Circuit Zero Crossing Detector 1

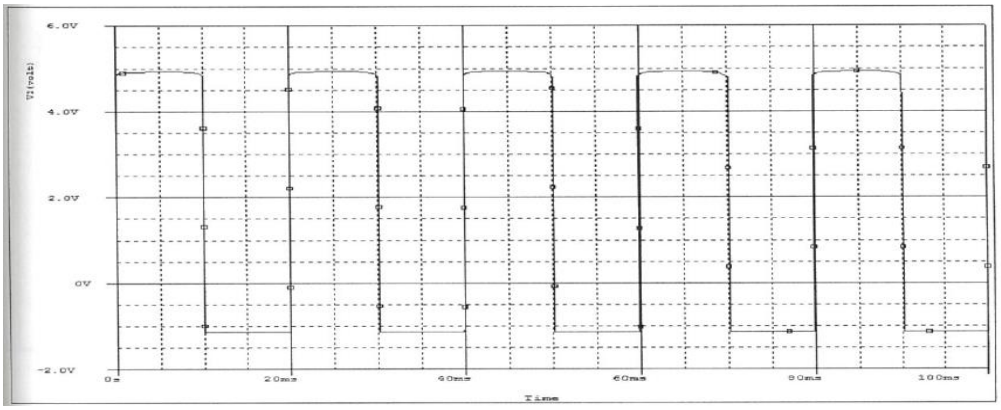


Fig.6 Simulation result of Zero Crossing Detector 1

Simulation of RC Differentiator 1

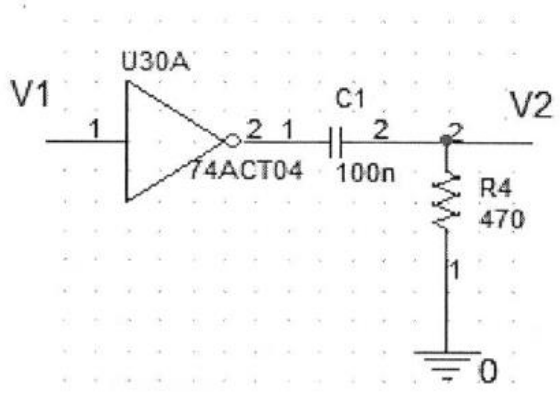


Fig.7 Simulation of PSpice Circuit RC differentiator1

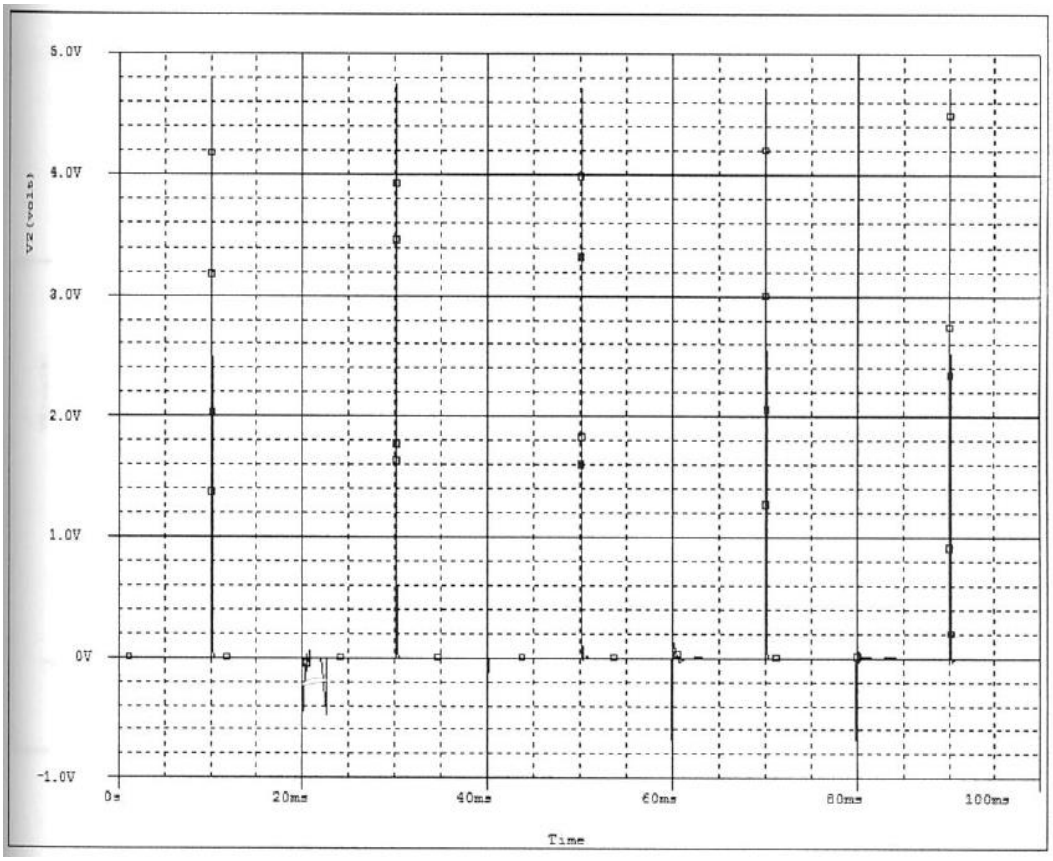
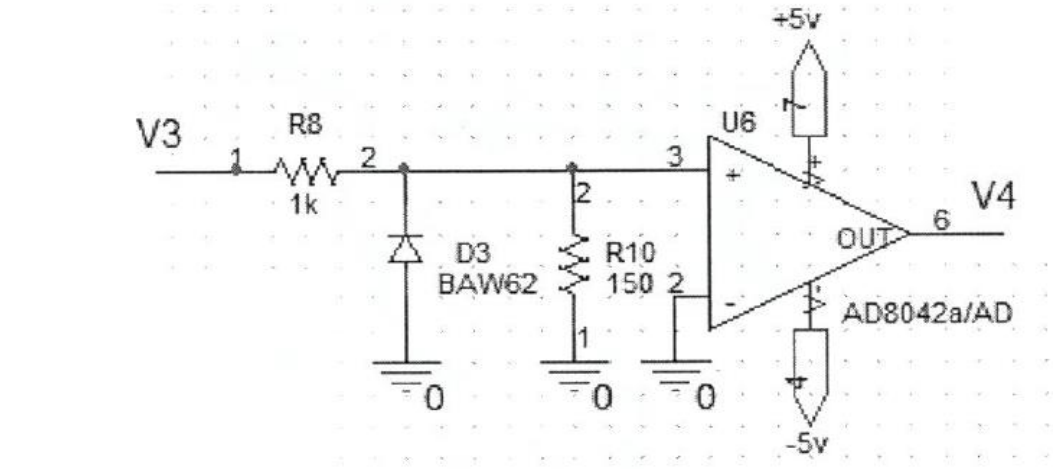


Fig.8 Simulation result of RC Differentiator

Simulation of Zero Crossing Detector 2



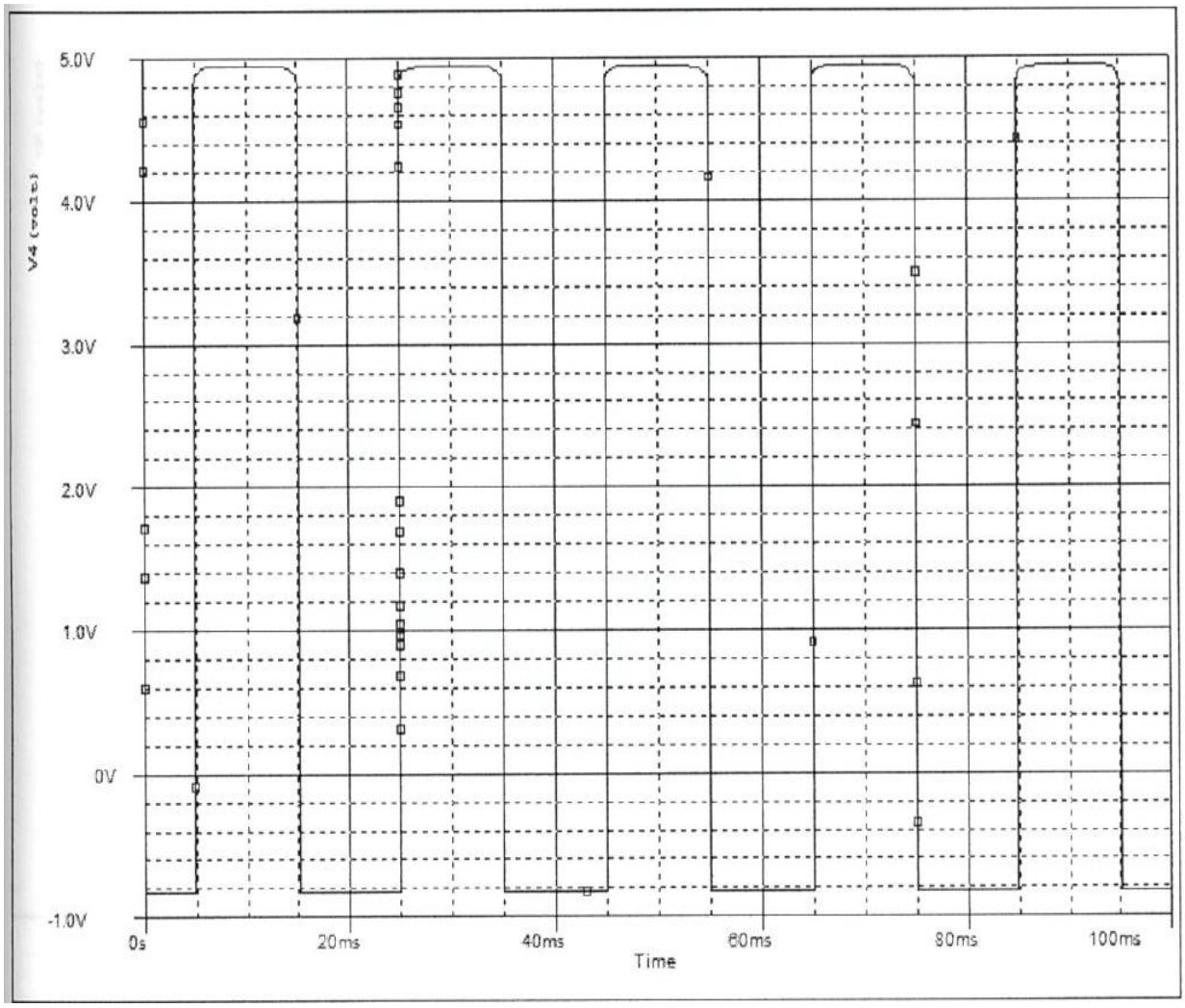


Fig.10 Simulation of pspice circuit and result of Zero Crossing Detector 2

Simulation Output for the Complete Circuit

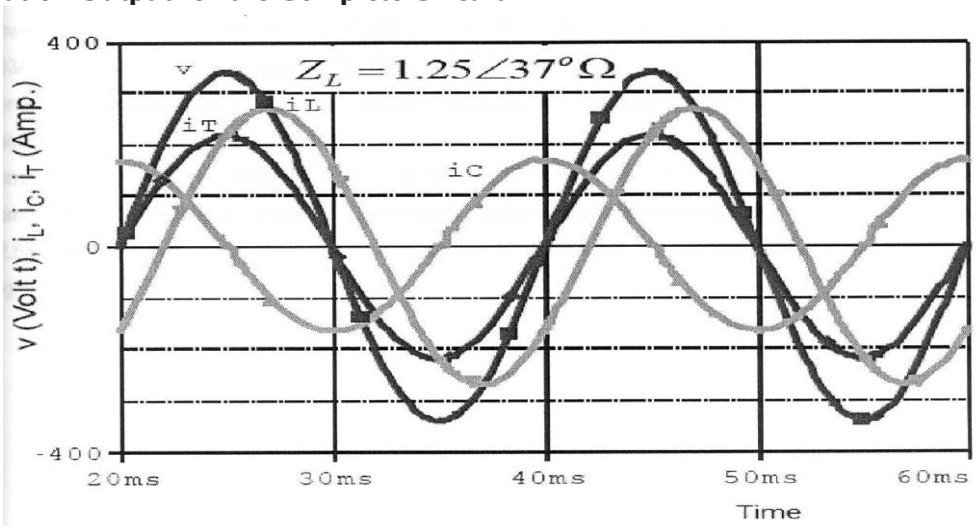


Fig.11 Simulation Output for Overall Circuit for unity power factor

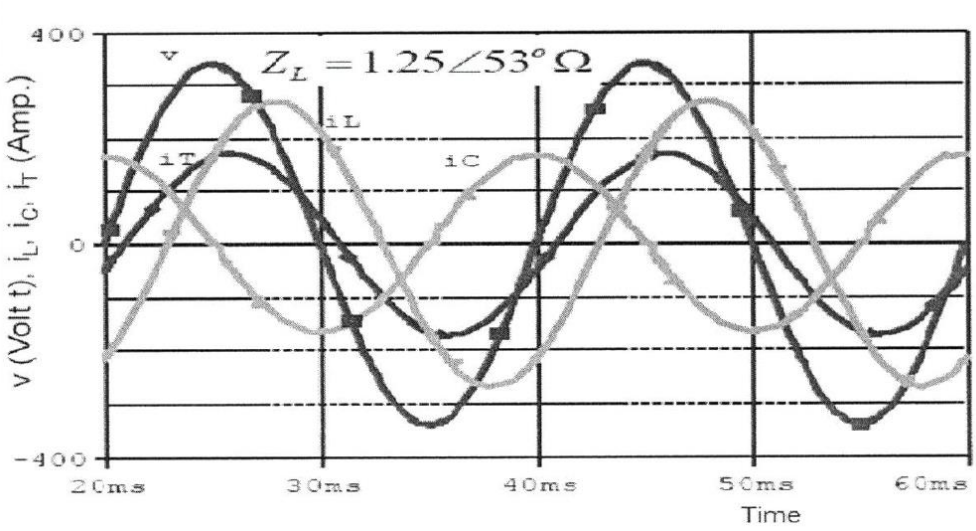


Fig.12 Simulation Output for Power Factor Improvement

Fig.4.5 shows PSpice tests for the single-phase system. The first test corresponds to the case at which the load impedance (ZL) was 1.25 ohm with power factor angle of 37°. The power factor for this load is 0.8 lagging. The reactive component of the load current was 163A (peak value) which was within the compensator rating. Consequently the compensator generated a capacitive reactive current completely cancelled the load current reactive component yielding a real total current UT) as shown in Fig.11. The second test corresponds to an inductive load of 1.25 ohm with power factor angle of 53°. The reactive component for that load was 217.6A (peak value) which exceeded the system rating by 52.6A (peak value). Therefore the power factor for that load was only improved as shown in Fig.12

5. CONCLUSION

The proposed single-phase automatic power factor correction system have certain reactive current or reactive power ratings. When the detected reactive power absorbed by the load is greater than the compensator rating, the power factor will not be corrected to unity, but certainly will be improved and the apparent power supplied by the ac supply will be reduced.

This system responds almost linearly throughout its pre-assigned areas of operation. It achieves better power quality by reducing the apparent power drawn from the ac supply and minimizing the power transmission losses. In addition, no harmonics disturbing the power system network are released, and hence no filtering is required. The response of the system is settled down within the power system network fundamental cycle. There is a feasibility of utilizing this technique for designing systems with high voltage and current ratings.

Since this technique is not dealt with accomplishing balanced three-phase currents, the future work will be extended to design an integrated system capable of achieving both power factor correction and load balancing in three phase systems.

6. REFERENCES

1. Aashish Goyal, NeharikaKapil,Sheila Mahapatra(2014), Implementation of Thyristor Switched Capacitors for Power Factor Improvement, Advance in Electronic and Electric Engineering.4(3),225-230.

2. Ashish Chandra , Taru Agarwal(2014), Power Factor Improvement of Induction Motor by Using Capacitors, International Journal of Emerging Technology and Advanced Engineering,4(8),pp.235-239.

3. Mr.Anant Kumar Tiwari, Mrs. Durga Sharma, Mr.Vijay Kumar Sharma(2014), Automatic Power Factor Correction Using Capacitive Bank, Int. Journal of Engineering Research and Applications,4(2),pp.393-395.

4. Muhammad Bilal Khan, Muhammad Owais(2016), International conference on Computing, Electronic and Electrical Engineering,11-12 april 2016.

5. Samarjit Bhattacharyya, Dr. A Choudhury, Prof H.R. Jariwala(2011), Case Study On Power Factor Improvement, International Journal of Engineering Science and Technology (IJEST),3(12),pp.8372-8378.

6. Aparna Sarkar, Umesh Hiwase(2015), Automatic Power Factor Correction by Continuous Monitoring, International Journal of Engineering and Innovative Technology,4(10),pp.170-176.

7. Myint Myint Than, Implementation of Power Factor Correction Using Solid State Switched Capacitors (2016), IOSR Journal of Electrical and Electronics Engineering,11(4),pp.70-79.